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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,173	YOUNG, NIGEL D.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8 and 13-15* is/are rejected.

7)☒ Claim(s) *3-7,9-12 and 19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Morozumi (U.S. 4,862,237). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

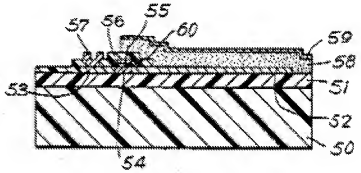
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morozumi ('237) in view of Kusumoto et al. (U.S. 6,027,960, hereinafter Kusumoto), Wolf et al. (Silicon Processing for the VLSI Era, Volume 1, Process technology, hereinafter Wolf) and Wei et al. (U.S. 5,480,810, hereinafter Wei).

In reference to claim 1, Morozumi (Figs.5) teaches a method of forming an image sensor thin film transistor including forming on a circuit substrate a crystalline active semiconductor film (52, 53, 54) of the transistor with a first process involving a first processing temperature; forming doped source and drain regions (52, 53) of the transistor at ends of a channel area (54) with a second process involving a second processing temperature; forming a dielectric layer (56) over the crystalline active semiconductor film (52, 53, 54); providing an interconnection film (52) between an

electrode area (55) of the transistor and a diode area over which a diode (58, 59) is to be formed; depositing the active semiconductor film (58) for the diode (58, 59) over the interconnection film (52) and the dielectric layer (56) with a third process that involves a third processing temperature; and leaving the active semiconductor film (58) for the diode (58, 59) over the interconnection film (52) in the diode area and over the dielectric layer (56), wherein the semiconductor film (58) for the diode (58, 59) is an amorphous silicon PIN diode (Morozumi, column 5, line 40 – column 6, line 57, see drawing below).



Second embodiment of Morozumi

Morozumi fails to expressly disclose a process temperature for the formation of the active crystalline semiconductor film.

However, Kusumoto (Figs.2A-2F) teaches a method of manufacturing thin-film transistor including the steps of forming on a circuit substrate the crystalline active semiconductor film (203) of the transistor with a first process involving a first processing temperature of 600°C; and forming doped source and drain regions (208, 209) of the transistor at ends of the channel area with a second process involving a second

processing temperature of 450°C (Kusumoto, column 7, lines 8 – 54 and column 11, lines 10 – 40).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Morozumi and Kusumoto to enable forming the crystalline active semiconductor film and the doped source and drain regions of Morozumi according to the teachings of Kusumoto because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed crystalline active semiconductor film and the doped source and drain regions of Morozumi and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, it would have been obvious to a person of ordinary skill in the art to try the process of Kusumoto to provide the disclosed crystalline active semiconductor film and the doped source and drain regions of Morozumi, as a person with ordinary skill has good reason to pursue the known options within his or her technical grasp. Since the process would lead to the anticipated semiconductor and the source and drain regions, it is likely a process not of innovation but of ordinary skill and common sense.

Still, the combined teachings of Morozumi and Kusumoto fail to disclose a deposition temperature for the PIN diode. However, the combined teachings of Morozumi and Kusumoto disclose wherein said PIN diode is made of amorphous silicon (Morozumi, column 6, lines 38 – 41). Taking this into consideration, Wolf discloses forming amorphous silicon at temperatures below 580°C (Wolf, page 179).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Morozumi and Kusumoto with Wolf to enable forming the amorphous silicon used for the PIN diode Morozumi and Kusumoto at the deposition temperatures disclosed in Wolf because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the diode of Morozumi and Kusumoto and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, the combination of Morozumi, Kusumoto and Wolf is open to form the crystalline active semiconductor film and the source and drain regions at temperatures higher than the temperature used to form the amorphous PIN diode. Therefore, one of ordinary skill in the art at the time the invention was made would have used the combination of Morozumi, Kusumoto and Wolf to arrive at the recited temperature differences.

Still, the combined teachings of Morozumi, Kusumoto and Wolf fail to disclose forming the PIN diode by depositing an active semiconductor film for the diode and etching away the active semiconductor film for the diode from over an etch-stop film to leave the active semiconductor film for the diode.

However, Wei (Figs.1a-1b) teaches a method of manufacturing thin-film circuit elements that include a diode (145) integrated with a crystalline thin-film transistor including the steps of forming a metal conductive region (120) over a substrate (105); etching said metal conductive region to form an electrode (124); forming an active

semiconductor film for the PIN diode (145) on said conductive region (120); and etching away the active semiconductor film for the PIN diode (145) stopping at the conductive region (120) and the substrate (105) to from said PIN diode (145) (Wei, column 3, line 47 – column 4, line 60).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Morozumi, Kusumoto and Wolf with Wei to enable forming the PIN diode over the interconnection structure of Morozumi, Kusumoto and Wolf according to the teachings of Wei because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed interconnection electrode of Morozumi, Kusumoto and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the underlying layer, in this case a dielectric layer, of the combination of Morozumi, Kusumoto and Wolf as taught by Wei because a person of ordinary skill has good reason to pursue the known options, in this case, an etching process to form the PIN diode, within his or her technical grasp. Since this leads to the anticipated PIN diode, it is likely the etching process is not a product not of innovation but of ordinary skill and common sense.

In reference to claim 2, the combined teachings of Morozumi, Kusumoto, Wolf and Wei teach wherein the etch-stop film is an insulating film that extends over the

interconnection film and that has a window at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode.

In reference to claim 14, the combined teachings of Morozumi, Kusumoto, Wolf and Wei teach wherein the crystalline semiconductor film is formed by a process including crystallizing a deposited semiconductor film using laser heating of the film (Kusumoto, column 7, lines 8 – 54).

In reference to claim 15, the combined teachings of Morozumi, Kusumoto, Wolf and Wei teach wherein the doped source and drain regions are formed by an ion implant of dopant in the crystalline semiconductor film and by annealing the implanted dopant (Kusumoto, column 11, lines 3 – 40).

4. Claims 1, 8, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonuk et al. (U.S. 5,079,426, hereinafter Antonuk) in view of Kusumoto ('960), Wolf (Silicon Processing for the VLSI Era) and Wei ('810).

Antonuk (Figs.1-2) teaches a method of manufacturing thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor (52) including the steps of forming on a circuit substrate (12) an active film (22, 25, 27, 28); forming doped source and drain regions (25, 29) of the transistor at ends of a channel area; providing an interconnection electrode film (22) between an electrode area of the thin film transistor (52) and a diode area over which the diode (30) on which the active film for the diode is to be deposited; and forming said diode (30) over the interconnection film (22), wherein the diode (30) is formed after forming the active film (22, 25, 27, 28),

wherein said diode (30) is a PIN diode, and wherein said thin film transistor is made of crystalline silicon (Antonuk, column 4, line 54 – column 6, line 10, see drawing below).

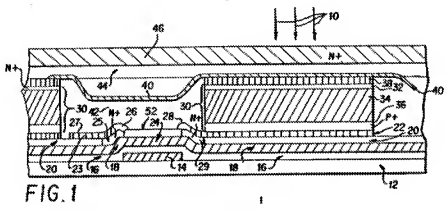


Image sensor device of Antonuk.

Antonuk fails to expressly disclose a process temperature for the formation of the active crystalline semiconductor film.

However, Kusumoto (Figs.2A-2F) teaches a method of manufacturing thin-film transistor including the steps of forming on a circuit substrate the crystalline active semiconductor film (203) of the transistor with a first process involving a first processing temperature of 600°C; and forming doped source and drain regions (208, 209) of the transistor at ends of the channel area with a second process involving a second processing temperature of 450°C (Kusumoto, column 7, lines 8 – 54 and column 11, lines 10 – 40).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Antonuk and Kusumoto to enable forming the crystalline active semiconductor film and the doped source and drain regions of Antonuk according to the

teachings of Kusumoto because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed crystalline active semiconductor film and the doped source and drain regions of Antonuk and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, it would have been obvious to a person of ordinary skill in the art to try the process of Kusumoto to provide the disclosed crystalline active semiconductor film and the doped source and drain regions of Antonuk, as a person with ordinary skill has good reason to pursue the known options within his or her technical grasp. Since the process would lead to the anticipated semiconductor and the source and drain regions, it is likely a process not of innovation but of ordinary skill and common sense.

Still, the combined teachings of Antonuk and Kusumoto fail to disclose a deposition temperature for the PIN diode. However, the combined teachings of Antonuk and Kusumoto disclose wherein said PIN diode is made of amorphous silicon (Antonuk, column 5, lines 17 – 25). Taking this into consideration, Wolf discloses forming amorphous silicon at temperatures below 580°C (Wolf, page 179).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Antonuk and Kusumoto with Wolf to enable forming the amorphous silicon used for the PIN diode of Antonuk and Kusumoto at the deposition temperatures disclosed in Wolf because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the diode of Antonuk and Kusumoto and art

recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, the combination of Antonuk, Kusumoto and Wolf is open to form the crystalline active semiconductor film and the source and drain regions at temperatures higher than the temperature used to form the amorphous PIN diode. Therefore, one of ordinary skill in the art at the time the invention was made would have used the combination of Antonuk, Kusumoto and Wolf to arrive at the recited temperature differences.

Still, the combined teachings of Antonuk, Kusumoto and Wolf fail to disclose forming the PIN diode by depositing an active semiconductor film for the diode and etching away the active semiconductor film for the diode from over an etch-stop film to leave the active semiconductor film for the diode.

However, Wei (Figs.1a-1b) teaches a method of manufacturing thin-film circuit elements that include a diode (145) integrated with a crystalline thin-film transistor including the steps of forming a metal conductive region (120) over a substrate (105); etching said metal conductive region to form an electrode (124); forming an active semiconductor film for the PIN diode (145) on said conductive region (120); and etching away the active semiconductor film for the PIN diode (145) stopping at the conductive region (120) and the substrate (105) to from said PIN diode (145) (Wei, column 3, line 47 – column 4, line 60).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Antonuk, Kusumoto and Wolf with Wei to enable the disclosed forming

the interconnection electrode and the PIN diode of Antonuk, Kusumoto and Wolf according to the teachings of Wei because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed interconnection electrode of Antonuk, Kusumoto and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the underlying layer, in this case, the electrode layer of the combination of Antonuk, Kusumoto and Wolf as taught by Wei because a person of ordinary skill has good reason to pursue the known options, in this case, an etching process to form the PIN diode, within his or her technical grasp. Since this leads to the anticipated PIN diode, it is likely the etching process is not a product not of innovation but of ordinary skill and common sense.

In reference to claim 8, the combined teachings of Antonuk, Kusumoto, Wolf and Wei teach wherein the interconnection film comprises a metal which provides the etch-stop, and the diode has a vertical PIN doped structure formed in its active semiconductor film as an intrinsic region between P and N electrode regions.

In reference to claim 14, the combined teachings of Antonuk, Kusumoto, Wolf and Wei teach wherein the crystalline semiconductor film is formed by a process including crystallizing a deposited semiconductor film using laser heating of the film (Kusumoto, column 7, lines 8 – 54).

In reference to claim 15, the combined teachings of Antonuk, Kusumoto, Wolf and Wei teach wherein the doped source and drain regions are formed by an ion implant of dopant in the crystalline semiconductor film and by annealing the implanted dopant (Kusumoto, column 11, lines 3 – 40).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morozumi ('237) in view of Kusumoto ('960), Wolf (Silicon Processing for the VLSI Era) and Wei ('810) as applied to claims 1 and 2 above, and further in view of Kitakado et al. (U.S. 7,176,068 B2, hereinafter Kitakado).

The combined teachings of Morozumi, Kusumoto, Wolf and Wei substantially teach all aspects of the invention but fail to dislcose wherein the crystalline semiconductor film is subjected to a hydrogenation process.

However, Kitakado (Figs.1A-4) teaches a method to form thin-film circuit elements that include a crystalline thin-film transistor including the steps of forming on a circuit substrate (101) a crystalline silicon active film (107), wherein said forming of said crystalline silicon active film further includes laser crystallization; forming a source/drain regions (113, 114) in the crystalline active film (107) involving temperatures between 300°C to 650°C; forming an insulating film (108) over said crystalline film (107); and performing a hydrogenation step to the crystalline active semiconductor film (107) (Kitakado, column 6, line 4 – column 8, line 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Morozumi, Kusumoto, Wolf and Wei to

enable performing the hydrogenation step on the active crystalline semiconductor film of Morozumi, Kusumoto, Wolf and Wei according to the teachings of Kitakado for the further advantage of terminating the dangling bonds in the active layer by thermally excited hydrogen (Kitakado, column 8, lines 50 – 65).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Antonuk ('426) in view of Kusumoto ('960), Wolf (Silicon Processing for the VLSI Era) and Wei ('810) as applied to claims 1 and 2 above, and further in view of Kitakado ('068).

The combined teachings of Antonuk, Kusumoto, Wolf and Wei substantially teach all aspects of the invention but fail to dislcose wherein the crystalline semiconductor film is subjected to a hydrogenation process.

However, Kitakado (Figs.1A-4) teaches a method to form thin-film circuit elements that include a crystalline thin-film transistor including the steps of forming on a circuit substrate (101) a crystalline silicon active film (107), wherein said forming of said crystalline silicon active film further includes laser crystallization; forming a source/drain regions (113, 114) in the crystalline active film (107) involving temperatures between 300°C to 650°C; forming an insulating film (108) over said crystalline film (107); and performing a hydrogenation step to the crystalline active semiconductor film (107) (Kitakado, column 6, line 4 – column 8, line 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Antonuk, Kusumoto, Wolf and Wei to enable performing the hydrogenation step on the active crystalline semiconductor film of

Antonuk, Kusumoto, Wolf and Wei according to the teachings of Kitakado for the further advantage of terminating the dangling bonds in the active layer by thermally excited hydrogen (Kitakado, column 8, lines 50 – 65).

Allowable Subject Matter

7. Claims 3-7, 9-12 and 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record teaches away from an active semiconductor film used to form the source and drain regions, an interconnection portion and a bottom one of the P and N electrode regions of the PIN diode as disclosed in claim 3.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to dislcose wherien at least a portion of the etch-stop interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a top gate electrode of the transistor which is interconnected with a bottom one of the P and N electrode regions of the PIN diode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is

(571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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